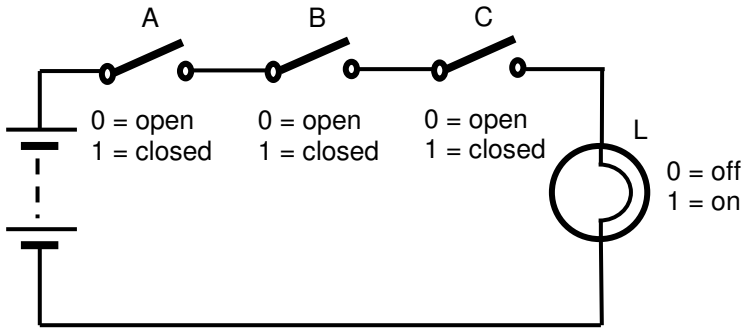
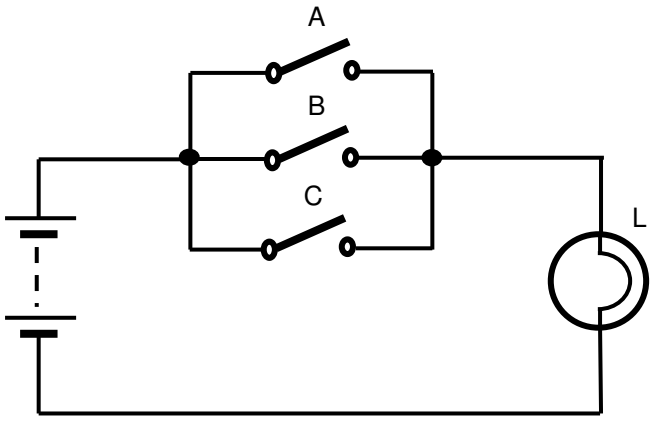
Answers to Exercises in Chapter 23

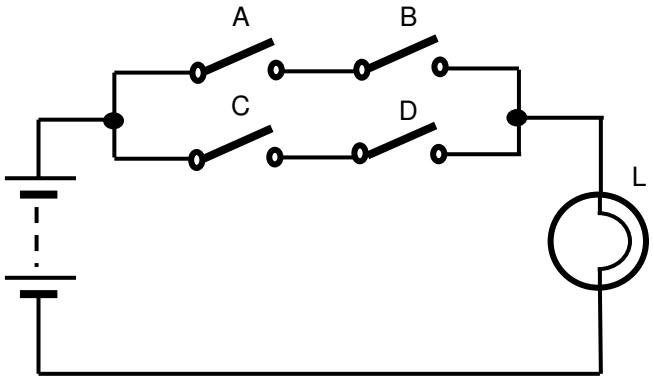
23.1 $L = A \cdot B \cdot C$



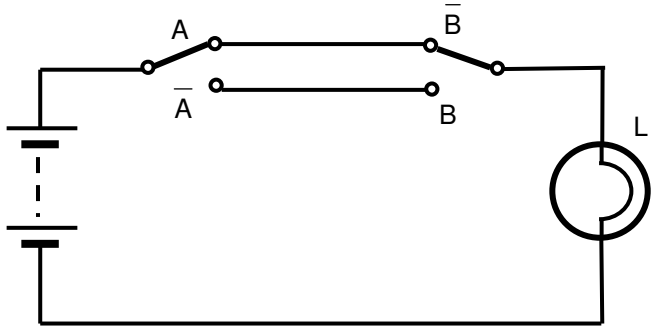
$L = A + B + C$



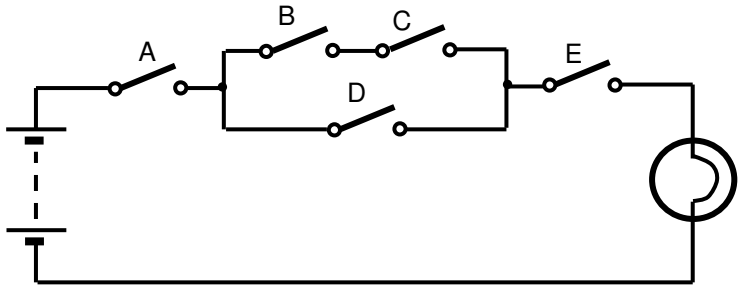
$L = (A \cdot B) + (C \cdot D)$



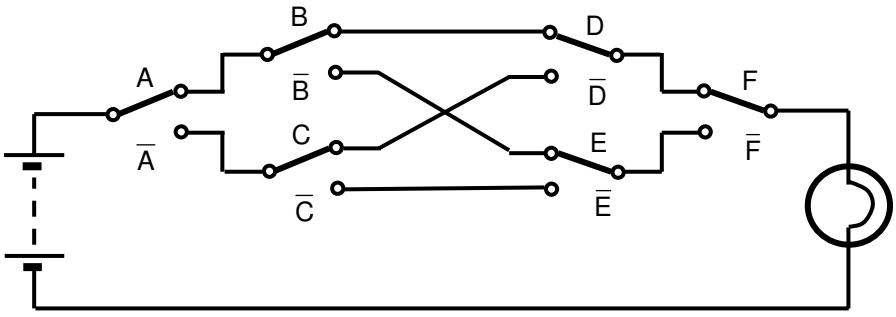
$L = A \oplus B$



23.2



By inspection the function is: $L = A$ AND ((B AND C) OR D) AND E



One of the purposes of this exercise is to show how cumbersome it is to describe complex expression in this way. Hence the advantage of Boolean Algebra. Here

L = (A AND B AND D AND F)
OR (A AND NOT B AND E AND NOT F)
OR (NOT A AND C AND NOT D AND F)
OR (NOT A AND NOT C AND NOT E AND NOT F)

23.3 The first has 5 variables and so would have $2^5 = 32$ rows. The second has 6 variables and so would have $2^6 = 64$ rows.

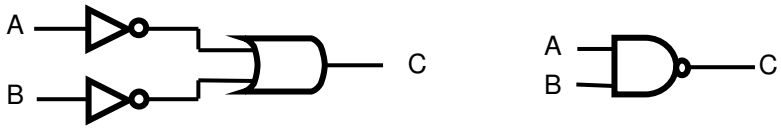
23.4 Truth table of a three-input NAND gate.

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

23.5 Truth table of a three input NOR gate.

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

23.6

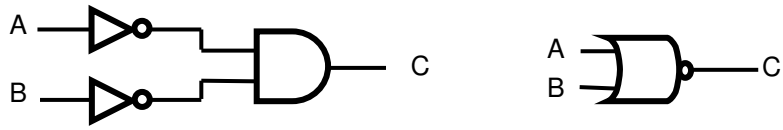


(a) (b)

Truth table for each is:

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

23.7



(a) (b)

Truth table for each is:

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

23.8 Circuits for these simulations can be easily produced by modifying the demonstration files for Computer Simulation Exercise 23.2.

23.9 The possible values of a Boolean constant are 0 and 1.

23.10 The possible values of a Boolean variable are 0 and 1.

23.11 The symbols are '•', '+', '$\overline{\ }$' and '$\oplus$' respectively.

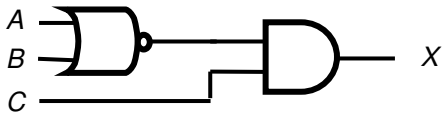
23.12 $X = \overline{(A + B + C)}$

23.13 $A \bullet 1 = A$; $A \bullet \overline{A} = 0$; $1 + A = 1$; $A + \overline{A} = 1$; $1 \bullet 0 = 0$; $1 + 0 = 1$.

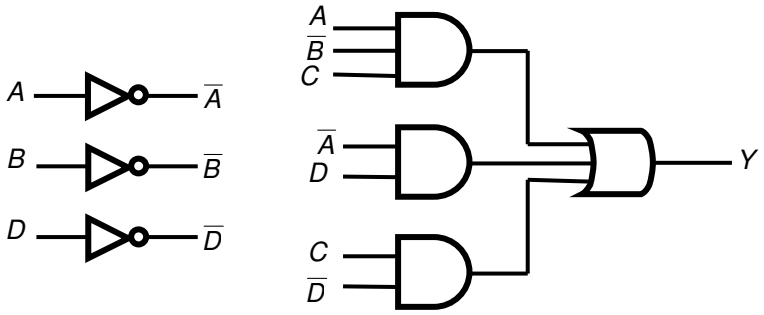
23.14 De Morgan's laws.

23.15 In combinational logic the outputs are determined solely by the current states of the inputs to the circuit. In sequential logic the outputs are determined not only by the current inputs, but also by the sequence of inputs that has led to the current state.

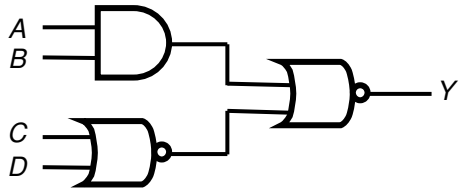
23.16 $X = \overline{(A + B)} \bullet C$



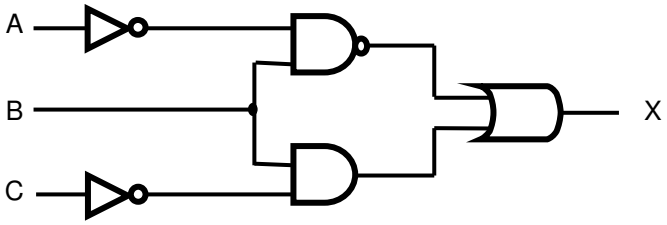
$Y = A\overline{B}C + \overline{A}D + C\overline{D}$



$Z = \overline{(A \bullet B) + \overline{(C + D)}}$



23.17



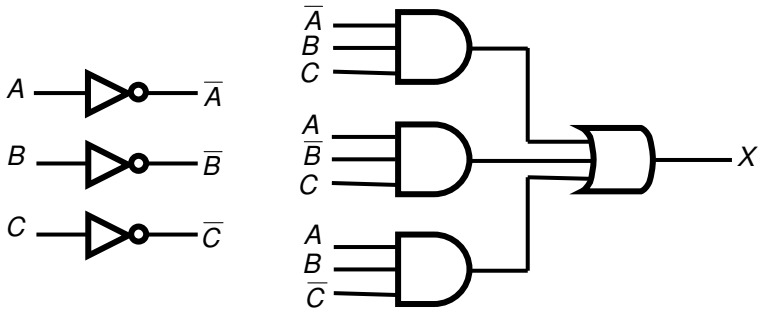
By inspection $X = \overline{\overline{A}B} + B\overline{C}$

23.18 Truth table.

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

By inspection $X = \overline{A}BC + A\overline{B}C + AB\overline{C}$

Which can be implemented as:



23.19 A circuit for this simulation can be easily produced by modifying the demonstration files for Computer Simulation Exercise 23.3.

23.20 From the diagram X is given by $A \bullet B$. This does not simplify.

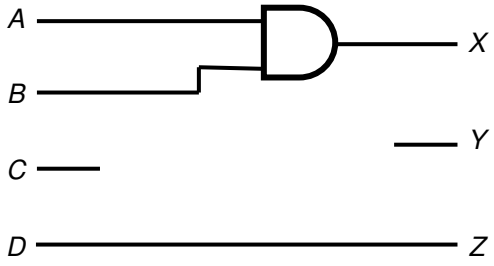
Y is given by the expression

$$Y = A \bullet B \bullet (\overline{B + C})$$
$$= A \bullet B \bullet (\overline{B} \bullet \overline{C}) = 0$$

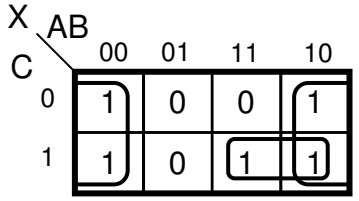
Thus Z is given by

$$Z = Y + D = 0 + D = D$$

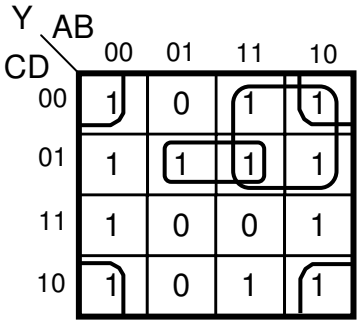
and therefore the arrangement may be simplified to



23.21

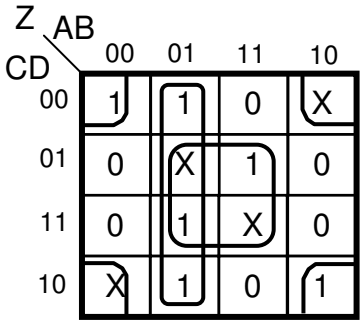


$$X = \overline{B} + AC$$



$$Y = \overline{B}\,\overline{D} + A\overline{C} + B\overline{C}D$$

23.22



$$Z = \overline{B}\,\overline{D} + BD + \overline{A}B$$

23.23 $1100 = 12_{10}$

$110001 = 49_{10}$

$10111 = 23_{10}$

$1.011 = 1.375$

23.24 $56 = 111000_2$

$132 = 10000100$

$67 = 1000011$

$5.625 = 101.101$

23.25 $A4C3_{16} = 42179_{10}$

$CB45_{16} = 52037_{10}$

$87_{16} = 135_{10}$

$3FF_{16} = 1023_{10}$

23.26 $52708_{10} = CDE4_{16}$

$726_{10} = 2D6_{16}$

$8900_{10} = 22C4_{16}$

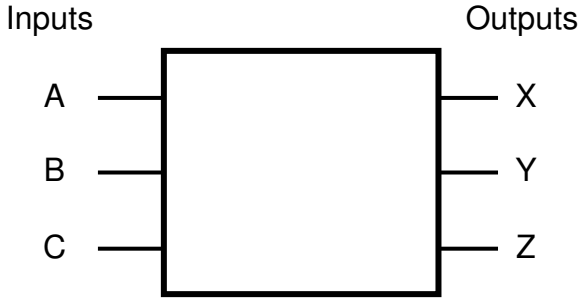
23.27 $A4C7_{16} = 1010\ 0100\ 1100\ 0111_2$.

23.28 $10110010100101_2 = 2CA5_{16}$

23.29

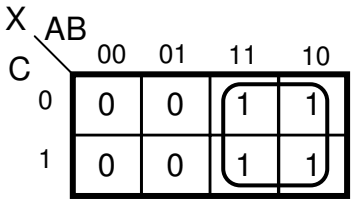
10111	110101	1011	101010
+1001	−11010	×111	÷110
100000	11011	1001101	111

23.30 The required system may be described by the following block diagram and truth table.

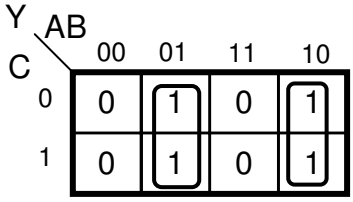


A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

From the truth table a series of Karnaugh maps may be formed and Boolean expressions found for the outputs.

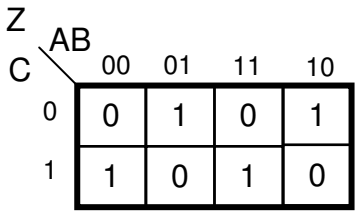


$X = A$



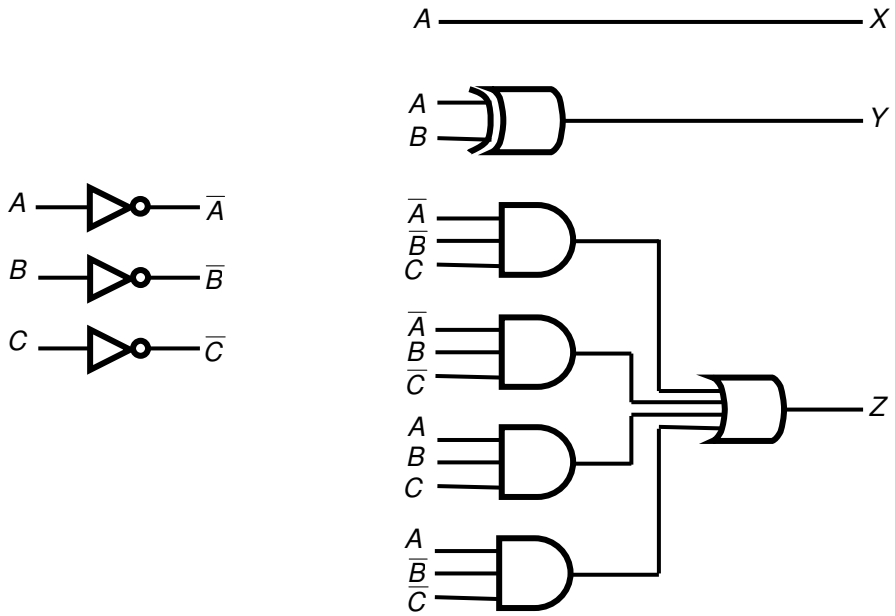
$Y = \overline{A}B + A\overline{B}$

$= A \oplus B$

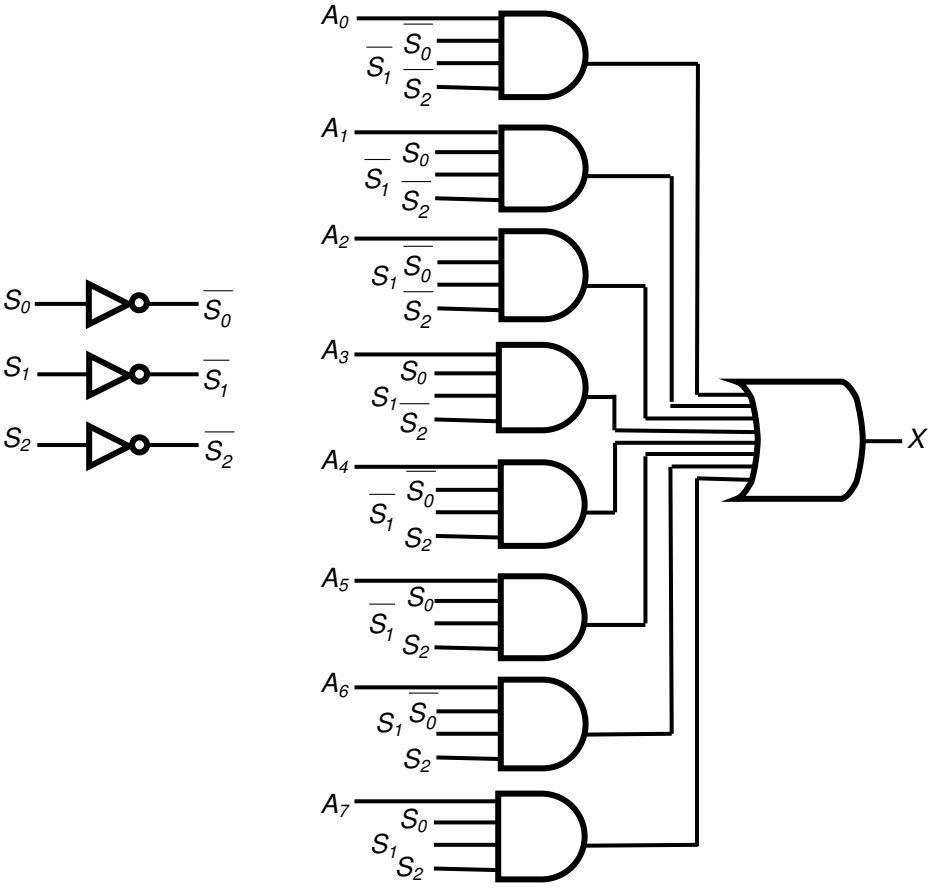


$Z = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + ABC + A\overline{B}\,\overline{C}$

From these expressions appropriate circuits may be designed.



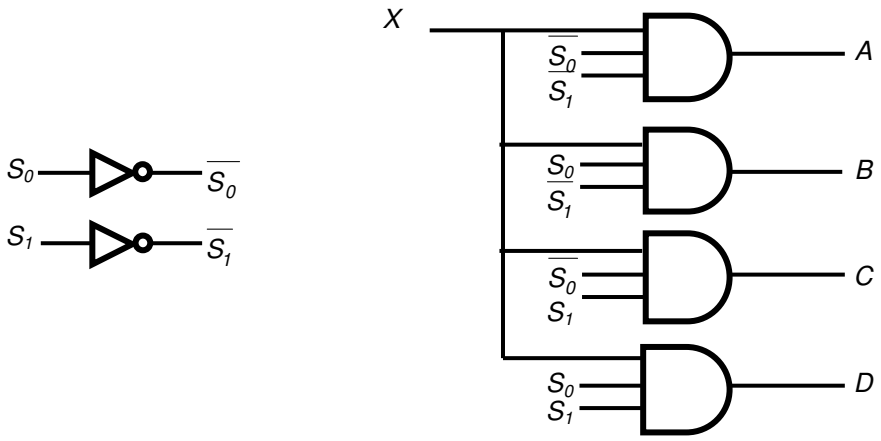
23.31 A suitable design is as follows.



23.32 The operation of this circuit can be demonstrated in a number of ways. Perhaps one of the most visual means is to adopt a similar approach to that used in computer simulation exercise 23.1 as demonstrated in FILE 23A.

If the simulation package you are using does not include an 8-input OR gate, this function must be produced using a combination of simpler gates. A resistor connected to ground must be connected to the output of the final gate to produce a voltage that can be displayed. A value of 10k is suitable.

23.33 A suitable design is as follows.



23.34 The operation of this circuit can be demonstrated in a number of ways. As described above for Exercise 23.32, perhaps one of the most visual means is to adopt a similar approach to that used in computer simulation exercise 23.1 as demonstrated in FILE 23A.

If the simulation package you are using does not include a 4 input OR gate, this function must be produced using a combination of simpler gates. Resistors to ground must be connected to the outputs of the output gates to produce voltages that can be displayed. A value of 10k is suitable.