Exercises

24.1 Explain the distinction between combinational and sequential logic.

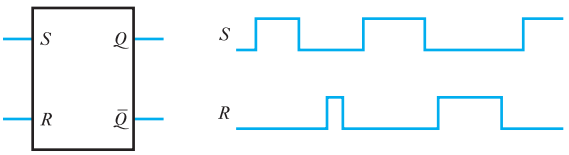
24.2 Define the terms 'bistable', 'monostable' and 'astable'.

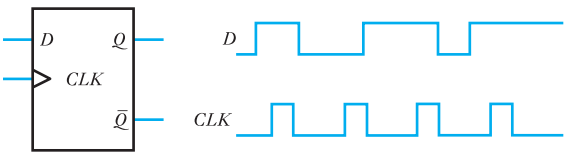
24.3 Explain the origins of the labels *S* and *R* given to the inputs of an S–R bistable.

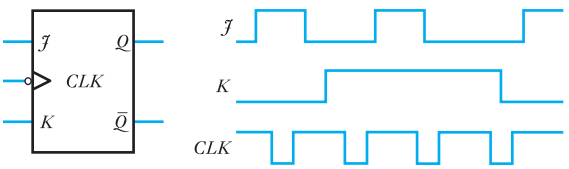
24.4 In an S–R bistable formed using two NOR gates, are the inputs active high or active low?

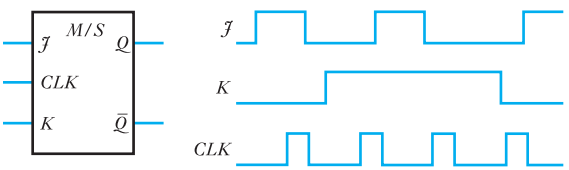
24.5 Under what circumstances does switch bounce cause problems in digital systems? Design a circuit using two input NOR gates to remove the effects of switch bounce from a changeover switch.

24.6 Deduce the waveform at the *Q* output of the following circuits.









24.7 What is meant by a race in sequential logic?

24.8 Explain how master/slave bistables overcome problems associated with races.

24.9 Explain the difference between a retriggerable and a non-retriggerable monostable.

24.10 What form of multivibrator has the characteristics of a digital oscillator?

24.11 Design an 8-bit memory register using D master/slave flip-flops, being careful to number your inputs and outputs appropriately.

24.12 Describe the operation of a simple shift register and explain how this can be used to perform serial to parallel and parallel to serial conversion.

24.13 Explain the meanings of the terms 'synchronous' and 'asynchronous' when applied to counters.

24.14 Design a modulo-5 ripple counter using negative edge-triggered J–K flip-flops.

24.15 Simulate your circuit for Exercise 24.14 and confirm that it functions as expected.

24.16 The decade counter in Figure 24.33 can be used to reduce the frequency of a clock waveform by a factor of 10 by taking the output from Q_3. For some applications, this has the disadvantage that the waveform produced is not a square wave. Design a 'divide by 10' counter that does produce a square-wave output. *Hint*: the circuit from the last exercise might be useful.

24.17 Simulate your solution to the previous exercise to confirm that the circuit functions as expected.

24.18 Design a modulo-10 ripple down counter using negative edge-triggered J–K bistables. The circuit should count down to 0 and then reset to 9.

24.19 Simulate your solution to the previous exercise to confirm that the circuit functions as expected.

24.20 Design a 4-bit up/down counter that does not overflow or underflow. That is, counting up is disabled when it reaches its maximum value and counting down is disabled when it reaches its minimum value. Can you think of any application for such a counter?

24.21 In Example 24.2 we looked at the design of a simple burglar alarm. Design a more sophisticated alarm that allows the houseowner to leave the house after turning the alarm on and to re-enter the house and turn the alarm off without it sounding. The unit should arm itself 30 seconds after a switch is closed and allow the user 30 seconds to turn it off before sounding the alarm.

24.22 Design a digital clock that displays the time in seconds, minutes and hours on six seven-segment displays. Your circuit should take into account the fact that such clocks display hours in the range 1 to 12, not 0 to 11.

24.23 Modify your design for Exercise 24.22 to allow the time to be set by depressing buttons to increment the seconds, minutes and hours settings.

24.24 Modify your design for Exercise 24.22 to allow the circuit to display time in either a 12-hour or 24-hour format. The display mode should be controlled by the setting of a switch.

24.25 Describe the effects of propagation delay on the maximum operating speed of a ripple counter. How are these problems tackled in a synchronous counter?